

Application No.: 09/875,197

Docket No.: 8733.132.20-US

AMENDMENTS TO THE CLAIMS

1-40. (Canceled)

41. (Current Amended): A method of fabricating a thin film transistor, comprising:
forming a gate insulating layer on an active layer;
forming a gate electrode on the gate insulating layer;
forming an excited region in an exposed portion of the active layer by implanting hydrogen ions to the active layer by using the gate as a mask, wherein said hydrogen ions are implanted with implantation energy between about 50 and about 150 KeV; and
forming an impurity region by implanting impurity ions to said excited region in a heavy dosage while the excited region remains in an excited state at a temperature between about 200 and about 300 degrees Celsius and has a temperature high enough to self-activate the impurity ions, whereby the implanted impurity ions become self-activated.
42. (Previously Presented): The method of claim 41, wherein the gate insulating layer is formed by depositing silicon dioxide or silicon nitride on a glass substrate.
43. (Previously Presented): The method of claim 41, wherein the active layer is formed by depositing undoped polycrystalline silicon.
44. (Previously Presented): The method of claim 43, wherein the undoped polycrystalline silicon has a thickness of between about 400 and 800 Å.
45. (Previously Presented): The method of claim 43, wherein the active layer is formed using chemical vapor deposition process.
46. (Previously Presented): The method of claim 41, wherein the active layer is formed by depositing amorphous silicon and crystallizing the amorphous silicon by laser annealing.
47. (Previously Presented): The method of claim 41, wherein the exposed portion of the active layer is formed by the steps of depositing an another layer of silicon dioxide on the gate

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insulating layer to cover the active layer; depositing a conductive material on the another layer of silicon dioxide; and patterning the conductive material and the another layer of silicon dioxide to form an insulating layer and to form the gate over a selected portion of the active layer.

48. (Previously Presented): The method of claim 47, wherein the gate insulating layer and the gate comprise a thickness of about 500-1500 Å and, about 1500-2500 Å, respectively.

49. (Cancelled)

50. (Previously Presented): The method of claim 41, wherein said hydrogen ions are implanted with a dose of between about 5×10^{14} - 5×10^{16} ions/cm².

51-52. (Cancelled)

53. (Previously Presented): The method of claim 41, wherein said hydrogen ions are implanted in the active layer and simultaneously form the impurity region.

54. (Previously Presented): The method of claim 41, wherein the hydrogen ion implantation time is proportionately related to the size of the active layer.

55. (Currently Amended): A thin film transistor prepared by a process comprising:
forming a gate insulating layer on an active layer;
forming a gate electrode on the gate insulating layer;
forming an excited region in an exposed portion of the active layer by implanting hydrogen ions to the active layer by using the gate as a mask, wherein said hydrogen ions are implanted with implantation energy between about 50 and about 150 KeV; and
forming an impurity region by implanting impurity ions to said excited region while the excited region remains in an excited state at a temperature between about 200 and about 300 degrees Celsius ~~and has a temperature high enough to self-activate the impurity ions~~, wherein the activation of said impurity ions implanted occurs as the step of said implanting impurity ions is performed.

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56. (Previously Presented): The thin film transistor of claim 55, wherein the gate insulating layer is formed by depositing silicon dioxide or silicon nitride on a glass substrate, and the active layer is formed by depositing undoped polycrystalline silicon.